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(54) **METHODS OF FORMING SEMICONDUCTOR DEVICES INCLUDING MESA STRUCTURES AND MULTIPLE PASSIVATION LAYERS AND RELATED DEVICES**

VERFAHREN ZUR HERSTELLUNG VON HALBLEITERVORRICHTUNGEN MIT MESASTRUKTUREN UND VIELFACHEN PASSIVIERUNGSSCHICHTEN UND VERWANDTE VORRICHTUNGEN

PROCEDE DE FABRICATION DE DISPOSITIFS A SEMICONDUCTEURS COMPRENANT DES STRUCTURES MESA ET DE MULTIPLES COUCHES DE PASSIVATION ET DISPOSITIFS ASSOCIES

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- **KOREN U ET AL: "INGAASP/INP UNDERCUT MESA LASER WITH PLANAR POLYIMIDE PASSIVATION" APPLIED PHYSICS LETTERS, AMERICAN INSTITUTE OF PHYSICS. NEW YORK, US, vol. 42, no. 5, March 1983 (1983-03), pages 403-405, XP000706209 ISSN: 0003-6951**

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Description

Related Applications

[0001] The present application claims the benefit of; U.S. Provisional Application No. 60/435,213 filed December 20, 2002, and entitled "*Laser Diode With Self-Aligned Index Guide And Via*"; U.S. Provisional Application No. 60/434,914 filed December 20, 2002, and entitled "*Laser Diode With Surface Depressed Ridge Waveguide*"; U.S. Provisional Application No. 60/434,999 filed December 20, 2002 and entitled "*Laser Diode with Etched Mesa Structure*"; and U.S. Provisional Application No. 60/435,211 filed December 20, 2002, and entitled "*Laser Diode With Metal Current Spreading Layer.*" The disclosures of each of these provisional applications are hereby incorporated herein in their entirety by reference.

[0002] The present application is also elated to: U.S. Application No._____ (Attorney Docket No. 5308-281) entitled "*Methods Of Forming Semiconductor Devices Having Self Aligned Semiconductor Mesas and Contact Layers And Related Devices*" filed concurrently herewith; U.S. Application No. _____ (Attorney Docket No. 5308-280) entitled "*Methods Of Forming Semiconductor Mesa Structures Including Self-Aligned Contact Layers And Related Devices*" filed concurrently herewith; and U.S. Application No._____ (Attorney Docket No. 5308-283) entitled "*Methods. Of Forming Electronic Devices Including Semiconductor Mesa Structures And Conductivity Junctions And Related Devices*" filed concurrently herewith. The disclosures of each of these U.S. Applications are hereby incorporated herein in their entirety by reference.

Field Of The Invention

[0003] The present invention relates to the field of electronics, and more particularly to methods of forming semiconductor devices and related structures.

Background

[0004] A laser is a device that produces a beam of coherent monochromatic light as a result of stimulated emission of photons. Stimulated emission of photons may also produce optical gain, which may cause light beams produced by lasers to have a high optical energy. A number of materials are capable of producing the lasing effect and include certain high-purity crystals (ruby is a common example), semiconductors, certain types of glass, certain gases including carbon dioxide, helium, argon and neon, and certain plasmas.

[0005] More recently, lasers have been developed in semiconducting materials, thus taking advantage of the smaller size, lower cost and other related advantages typically associated with semiconductor devices. In the semiconductor arts, devices in which photons play a major role are referred to as "photonic" or "optoelectronic" devices. In turn, photonic devices include light-emitting diodes (LEDs), photodetectors, photovoltaic devices, and semiconductor lasers.

[0006] Semiconductor lasers are similar to other lasers in that the emitted radiation has spatial and temporal coherence. As noted above, laser radiation is highly monochromatic (i.e., of narrow band width) and it produces highly directional beams of light. Semiconductor lasers may differ, however, from other lasers in several respects. For example, in semiconductor lasers, the quantum transitions are associated with the band properties of materials; semiconductor lasers may be very compact in size, may have very narrow active regions, and larger divergence of the laser beam; the characteristics of a semiconductor laser may be strongly influenced by the properties of the junction medium; and for P-N junction lasers, the lasing action is produced by passing a forward current through the diode itself. Overall, semiconductor lasers can provide very efficient systems that may be controlled by modulating the current directed across the devices. Additionally, because semiconductor lasers can have very short photon lifetimes, they may be used to produce high-frequency modulation. In turn, the compact size and capability for such high-frequency modulation may make semiconductor lasers an important light source for optical fiber communications.

[0007] In broad terms, the structure of a semiconductor laser should provide optical confinement to create a resonant cavity in which light amplification may occur, and electrical confinement to produce high current densities to cause stimulated emission to occur. Additionally, to produce the laser effect (stimulated emission of radiation), the semiconductor may be a direct bandgap material rather than an indirect bandgap material. As known to those familiar with semiconductor characteristics, a direct bandgap material is one in which an electron's transition from the valence band to the conduction band does not require a change in crystal momentum for the electron. Gallium arsenide and gallium nitride are examples of direct bandgap semiconductors. In indirect bandgap semiconductors, the alternative situation exists; i.e., a change of crystal momentum is required for an electron's transition between the valence and conduction bands. Silicon and silicon carbide are examples of such indirect semiconductors.

[0008] A useful explanation of the theory, structure and operation of semiconductor lasers, including optical and electronic confinement and mirroring, is given by Sze, Physics of Semiconductor Devices, 2nd Edition (1981) at pages 704-742, and these pages are incorporated entirely herein by reference.

[0009] As known to those familiar with photonic devices such as LEDs and lasers, the frequency of electromagnetic radiation (i.e., the photons) that can be produced by a given semiconductor material may be a function of the material's bandgap. Smaller bandgaps pro-

duce lower energy, longer wavelength photons, while wider bandgap materials produce higher energy, shorter wavelength photons. For example, one semiconductor commonly used for lasers is aluminum indium gallium phosphide (AlInGaP). Because of this material's bandgap (actually a range of bandgaps depending upon the mole or atomic fraction of each element present), the light that AlInGaP can produce may be limited to the red portion of the visible spectrum, i.e., about 600 to 700 nanometers (nm). In order to produce photons that have wavelengths in the blue or ultraviolet portions of the spectrum, semiconductor materials having relatively large bandgaps may be used. Group III-nitride materials such as gallium nitride (GaN), the ternary alloys indium gallium nitride (InGaN), aluminum gallium nitride (AlGaN) and aluminum indium nitride (AlInN) as well as the quaternary alloy aluminum gallium indium nitride (AlInGaN) are attractive candidate materials for blue and UV lasers because of their relatively high bandgap (3.36 eV at room temperature for GaN). Accordingly, Group III-nitride based laser diodes have been demonstrated that emit light in the 370-420 nm range.

[0010] A number of commonly assigned patents and co-pending patent applications likewise discuss the design and manufacture of optoelectronic devices. For example, U.S. Patent Nos. 6,459,100; 6,373,077; 6,201,262; 6,187,606; 5,912,477; and 5,416,342 describe various methods and structures for gallium-nitride based optoelectronic devices. U.S. Patent No. 5,838,706 describes low-strain nitride laser diode structures. Published U.S. Application Nos. 20020093020 and 20020022290 describe epitaxial structures fur nitride-based optoelectronic devices. Various metal contact structures and bonding methods, including flip-chip bonding methods, are described in Published U.S. Application No. 20020123164 as well as Published U.S. Application No. 030045015 entitled "Flip Chip Bonding of Light Emitting Devices and Light Emitting Devices Suitable for Flip-Chip Bonding"; Published U.S. Application No. 20030042507 entitled "Bonding of Light Emitting Diodes Having Shaped Substrates and Collets for Bonding of Light Emitting Diodes Having Shaped Substrates", and Published U.S. Application No. 20030015721 entitled "Light Emitting Diodes Including Modifications for Submount Bonding and Manufacturing Methods Therefor." Dry etching methods are described in U.S. Patent No. 6,475,889. Passivation methods for nitride optoelectronic devices are described in U.S. Application Ser. No. 08/920,409 entitled "Robust Group III Light Emitting Diode for High Reliability in Standard Packaging Applications" and Published U.S. Application No. 20030025121 entitled "Robust Group III Light Emitting Diode for High Reliability in Standard Packaging Applications." WO-A-01/95446 discloses a similar conventional method of manufacture. Active layer structures suitable for use in nitride laser diodes are described in Published U.S. Application No. 20030006418 entitled "Group III Nitride Based Light Emitting Diode Structures with a Quantum Well and Superlattice, Group III Nitride Based Quantum Well Structures and Group III Nitride Based Superlattice Structures" and Published U.S. Application No. 20030020061 entitled "Ultraviolet Light Emitting Diode." The contents of all of the foregoing patents, patent applications and published patent applications are incorporated entirely herein by reference as if fully set forth herein.

[0011] Stress and/or pressure applied to a surface of an electronic device including a semiconductor laser may damage a semiconductor structure providing the laser and/or electrical couplings therewith.

Summary

[0012] According to embodiments of the present invention, methods of forming semiconductor devices may include forming a semiconductor structure on a substrate wherein the semiconductor structure defines a mesa having a mesa surface opposite (i.e. remote from) the substrate and mesa sidewalls between the mesa surface and the substrate. A first passivation layer may be formed on at least portions of the mesa sidewalls and on the substrate adjacent the mesa sidewalls wherein at least a portion of the mesa surface is free of the first passivation layer and wherein the first passivation layer comprises a first material. In addition, a second passivation layer may be formed on the first passivation layer wherein at least a portion of the mesa surface is free of the second passivation layer, and wherein the second passivation layer comprises a second material different than the first material.

[0013] Moreover, at least a portion of the first passivation layer adjacent the mesa surface may be free of the second passivation layer, and a combined thickness of the first and second passivation layers may be greater than a thickness of the mesa. More particularly, a thickness of the first passivation layer may be greater than a thickness of the mesa. In addition, a contact layer may be formed on a portion of the mesa surface free of the first and second passivation layers, and a metal layer may be formed on the contact layer wherein the metal layer extends on at least a portion of the second passivation layer opposite the substrate. Moreover, the metal layer and the contact layer may comprise different materials.

[0014] A portion of the first passivation layer may extend on a portion of a surface of the contact layer opposite the substrate, or in an alternative, a portion of the contact layer may extend on a portion of at least one of the first and/or second passivation layers opposite the substrate. The first material may include aluminum oxide, and the second material may include silicon nitride. In addition, the semiconductor structure may include a P-type layer and an N-type layer wherein at least a portion of the P-type layer and/or N-type layer is included the mesa.

[0015] At least a portion of the mesa surface may be free of the first passivation layer before forming the sec-

ond passivation layer. More particularly, the second passivation layer may be formed on the first passivation layer and on the at least a portion of the mesa surface free of the first passivation layer. In addition, a hole may be formed in a portion of the second passivation layer exposing the at least a portion of the mesa surface free of the first passivation layer and exposing portions of the first passivation layer adjacent the mesa surface.

[0016] Moreover, the first passivation layer may be formed across the mesa surface, and the second passivation layer may be formed across the mesa surface so that the first and second passivation layers are both stacked across the mesa surface. A hole may then be formed in the second passivation layer exposing portions of the first passivation layer opposite the mesa surface, and after forming the hole in the second passivation layer, another hole may be formed in the first passivation layer exposing the at least a portion of the mesa surface. Before forming the first passivation layer, a contact layer may be formed on the mesa surface. In an alternative, a contact layer may be formed on at least portions of the mesa surface free of the first and second passivation layers after forming the second passivation layer.

[0017] Preferably, forming the hole in the portion of the second passivation layer comprises etching the second passivation layer using an etch chemistry that etches the second material of the second passivation layer preferentially with respect to the first material of the first passivation layer.

[0018] Alternatively, forming the first passivation layer is preceded by: forming a contact layer on the mesa surface, or forming the second passivation layer is followed by: forming a contact layer on at least portions of the mesa surface free of the first and second passivation layers.

[0019] According to additional embodiments of the present invention, methods of forming semiconductor devices may include forming a semiconductor structure on a substrate wherein the semiconductor structure defines a mesa having a mesa surface and mesa sidewalls between the mesa surface and the substrate. A passivation layer may be formed on the mesa sidewalls and on the substrate adjacent the mesa sidewalls, and the passivation layer may have a via hole therein so that at least a portion of the mesa surface is free of the passivation layer. More particularly, the via hole may define a stair-step profile such that a first portion of the via hole has a first width and a second portion of the via hole has a second width different than the first width.

[0020] The stair-step profile may include a plateau region between the first and second portions of the via hole having the first and second widths, and the plateau portion may be substantially parallel to the substrate. The first portion of the via hole having the first width may be between the second portion of the via hole having the second width and the mesa surface, and the second width may be greater than the first width. The passivation layer may include a first layer of a first material and second layer of a second material different than the first material, and the first portion of the via hole may be through at least a portion of the first layer and the second portion of the via hole may be through at least a portion of the second layer. More particularly, a thickness of the first passivation layer may be greater than a thickness of the mesa. In addition, the first material may include aluminum oxide, and the second material may include silicon nitride.

[0021] A contact layer may also be formed on the at least a portion of the mesa surface free of the passivation layer, and a metal layer may be formed on the contact layer and on at least portions of the passivation layer. The contact layer and the metal layer may comprise different materials, and a portion of the passivation layer may extend on a portion of the contact layer opposite the mesa surface. In an alternative, the contact layer may extend onto at least a portion of the passivation layer opposite the substrate. Moreover, the semiconductor structure may include a P-type layer and an N-type layer wherein at least a portion of the P-type layer and/or the N-type layer is included in the mesa.

[0022] According to still additional embodiments of the present invention, a semiconductor device includes a semiconductor structure on a substrate wherein the semiconductor structure defines a mesa having a mesa surface and mesa sidewalls between the mesa surface and the substrate. A first passivation layer is on at least portions of the mesa sidewalls and on the substrate adjacent the mesa sidewalls wherein at least a portion of the mesa surface is free of the first passivation layer and wherein the first passivation layer comprises a first material. A second passivation layer is on the first passivation layer wherein at least a portion of the mesa surface is free of the second passivation layer, and wherein the second passivation layer comprises a second material different than the first material.

[0023] At least a portion of the first passivation layer adjacent the mesa surface may be free of the second passivation layer, and a combined thickness of the first and second passivation layers may be greater than a thickness of the mesa. Moreover, a thickness of the first passivation layer may be greater than a thickness of the mesa.

[0024] The semiconductor device may also include a contact layer on a portion of the mesa surface free of the first and second passivation layers, and a metal layer on the contact layer wherein the metal layer extends on at least a portion of the second passivation layer opposite the substrate. Moreover, the metal layer and the contact layer may comprise different materials. A portion of the first passivation layer may extend on a portion of a surface of the contact layer opposite the substrate, or in an alternative, a portion of the contact layer may extend on a portion of at least one of the first and/or second passivation layers opposite the substrate.

[0025] The first material of the first passivation layer may comprise aluminum oxide, and the second material

of the second passivation layer may comprise silicon nitride. In addition, the semiconductor structure may include a P-type layer and an N-type layer wherein at least a portion of the P-type layer and/or N-type layer is included the mesa. Moreover, the first and second passivation layers may define a stair-step profile adjacent the at least a portion of the mesa surface free of the first and second passivation layers.

[0026] Preferably, the second material comprises a material that can be etched preferentially with respect to the first material using a predetermined etch chemistry.

[0027] According to yet additional embodiments of the present invention, a semiconductor device may include a semiconductor structure on a substrate wherein the semiconductor structure defines a mesa having a mesa surface and mesa sidewalls between the mesa surface and the substrate. The semiconductor device may also include a passivation layer on the mesa sidewalls and on the substrate adjacent the mesa sidewalls. More particularly, the passivation layer may have a via hole therein so that at least a portion of the mesa surface is free of the passivation layer wherein the via hole defines a stair-step profile such that a first portion of the via hole has a first width and a second portion of the via hole has a second width different than the first width.

[0028] The stair-step profile may include a plateau region between the first and second portions of the via hole having the first and second widths, and the plateau portion may be substantially parallel to the substrate. In addition, the first portion of the via hole having the first width may be between the second portion of the via hole having the second width and the mesa surface and the second width may be greater than the first width.

[0029] The passivation layer may include a first layer of a first material and second layer of a second material different than the first material with the first portion of the via hole being through at least a portion of the first layer and with the second portion of the via hole being through at least a portion of the second layer. A thickness of the first passivation layer may be greater than a thickness of the mesa, the first material of the first passivation layer may comprise aluminum oxide, and the second material of the second passivation layer may comprise silicon nitride.

[0030] The semiconductor device may also include a contact layer on the at least a portion of the mesa surface free of the passivation layer and a metal layer on the contact layer and on at least portions of the passivation layer, and the contact layer and the metal layer may comprise different materials. A portion of the passivation layer may extend on a portion of the contact layer opposite the mesa surface, or in an alternative, the contact layer may extend onto at least a portion of the passivation layer opposite the substrate. In addition, the semiconductor structure may includes a P-type layer and an N-type layer wherein at least a portion of the P-type layer and/or the N-type layer is included in the mesa.

Brief Description Of The Drawings

[0031]

Figure 1 is a cross-sectional view illustrating semiconductor devices according to embodiments of the present invention.

Figures 2A-2D are cross-sectional views illustrating steps of forming semiconductor devices according to embodiments of the present invention.

Figure 3 is a scanning electron microscope (SEM) photomicrograph of a semiconductor device according to embodiments of the present invention.

Figure 4 is a cross-sectional view illustrating semiconductor devices according to additional embodiments of the present invention.

Figures 5A-5D are cross-sectional views illustrating steps of forming semiconductor devices according to yet additional embodiments of the present invention.

Detailed Description

[0032] The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. The invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. It will also be understood that when a layer is referred to as being "on" another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present. It will also be understood that when an element is referred to as being "coupled" or "connected" to another element, it can be directly coupled or connected to the other element, or intervening elements may also be present. Like numbers refer to like elements throughout. Furthermore, relative terms such as "vertical" and "horizontal" may be used herein to describe a relationship with respect to a substrate or base layer as illustrated in the figures. It will be understood that these terms are intended to encompass different orientations of the device in addition to the orientation depicted in the figures.

[0033] Group III-V materials such as Group III-nitride materials may be made P-type by doping them with P-type impurities such as magnesium. However, P-type nitride semiconductors may have relatively low carrier activation rates and relatively low carrier mobilities. Accordingly, P-type nitride semiconductor materials may have relatively high resistivities. Because laser diodes may require relatively high current levels to provide conditions for lasing, it may be beneficial for an ohmic contact to a P-type nitride material to cover as much surface area as

possible.

[0034] Formation of laser diodes may include etching a mesa stripe into an epitaxial layer of a semiconductor material. Because the mesa stripe may be relatively narrow (on the order of approximately 2 microns in width), the mesa stripe may not have a high degree of mechanical stability, and the mesa stripe may be damaged relatively easily during subsequent fabrication steps such as bar coating, die attach, wafer bonding, etc. A mesa stripe may be formed within a trench of the semiconductor material and/or substrate with the trench having a depth greater than or equal to the height of the mesa to provide mechanical stability and/or protection.

[0035] As shown in Figure 1, structures according to embodiments of the present invention may provide mechanical protection for a semiconductor mesa stripe. Moreover, the structure of Figure 1 may be fabricated using steps that may be relatively repeatable and accurate. According to embodiments of the present invention, a semiconductor device may include a substrate **12**, an epitaxial semiconductor structure **14** including a mesa **20**, a first passivation layer **30**, a second passivation layer **40**, ohmic contact layers **26** and **27**, and a metal overlayer **50**. Moreover, the epitaxial semiconductor structure **14** may include a Group III-V compound semiconductor material such as a Group III-nitride compound semiconductor material. The ohmic contact layers **26** and **27** may each comprise a layer of a metal such as nickel, titanium, platinum, and/or palladium. The metal overlayer **50** may comprise a layer of a metal such as nickel, gold, platinum, titanium, tungsten, molybdenum, tantalum, and/or palladium.

[0036] In some embodiments, the substrate **12** may include substrate materials such as N-type silicon carbide having a polytype such as 2H, 4H, 6H, 8H, 15R, and/or 3C; sapphire; gallium nitride; and/or aluminum nitride. Moreover, the substrate **12** may be conductive to provide a "vertical" device having a "vertical" current flow through the epitaxial semiconductor structure **14** and the substrate **12**. In an alternative, the substrate **12** may be insulating or semi-insulating where both ohmic contacts are provided on a same side of the substrate to provide a "horizontal" device. A conductive substrate could also be used in a "horizontal" device. Moreover, the term substrate may be defined to include a non-patterned portion of the semiconductor material making up the semiconductor structure **14**, and/or there may not be a material transition between the substrate **12** and the semiconductor structure **14**.

[0037] Portions of the epitaxial semiconductor structure **14** may be patterned into a mesa stripe, for example, to provide optical and/or current confinement. As shown, only a portion of the epitaxial semiconductor structure **14** is included in the mesa **20**. For example, the epitaxial semiconductor structure **14** may include N-type and P-type layers and portions of one or both of the N-type and P-type layers may be included in the mesa **20**. According to particular embodiments, the epitaxial semiconductor structure **14** may include an N-type layer adjacent the substrate **12** and a P-type layer on the N-type layer opposite the substrate **12**. The mesa may include portions of the P-type layer and none of the N-type layer; all of the P-type layer and portions (but not all) of the N-type layer; or all of the P-type and N-type layers (such that sidewalls of the mesa **20** extend to the substrate **12**).

[0038] As discussed in greater detail in U.S. Application Serial No._____ (Attorney Docket No. 5308-281) filed concurrently herewith, a uniformly thick layer of the epitaxial semiconductor material may be formed, and the mesa **20** may be formed by selectively etching the epitaxial semiconductor material. Moreover, a thickness of the mesa **20** may be determined by a depth of the etch used to form the mesa. According to embodiments of the present invention, the mesa etch depth (and resulting mesa thickness) may be in the range of approximately 0.1 to 5 microns, and according to additional embodiments may be no greater than approximately 2.5 microns. In addition, a width of the mesa surface **20A** between mesa sidewalls may be in the range of approximately 1 to 3 microns. As shown in Figure 1, the ohmic contact layer **26** may be formed on a portion of the mesa surface **20A**. Moreover, the surface portion of the mesa may be a P-type semiconductor material.

[0039] The first passivation layer **30** may protect and insulate the epitaxial semiconductor structure **14** including the mesa **20**. The first passivation layer **30**, for example, may include a layer of an insulating material such as silicon dioxide, silicon nitride, aluminum oxide, and/or combinations thereof, and the first passivation layer **30** may be formed using a deposition technique such as plasma enhanced chemical vapor deposition (PECVD), low pressure chemical vapor deposition (LPCVD), chemical vapor deposition (CVD), sputtering, and/or e-beam evaporation. Moreover, the first passivation layer may be fabricated as discussed, for example, in U.S. Application Ser. No._____ (Attorney Docket No. 5308-280) filed concurrently herewith, and/or in U.S. Application Ser. No._____ (Attorney Docket No. 5308-281) filed concurrently herewith. The disclosures of both of these applications are incorporated herein in their entirety by reference.

[0040] The second passivation layer **40**, for example, may include a layer of an insulating material such as silicon dioxide, silicon nitride, aluminum oxide and/or combinations thereof, and the second passivation layer may be formed using a deposition technique such as plasma enhanced chemical vapor deposition (PECVD), low pressure chemical vapor deposition (LPCVD), chemical vapor deposition (CVD), sputtering, and/or e-beam evaporation. According to particular embodiments of the present invention, the first passivation layer may be formed of a first material, and the second passivation layer may be formed of a second material different than the first material. Accordingly, the first passivation layer may provide an etch selectivity with respect to the second passivation layer for one or more etch chemistries. Stated

in other words, the second passivation layer **40** may be more susceptible to certain etch chemistries than the first passivation layer so that a via hole **42** can be formed in the second passivation layer without significantly etching the first passivation layer. According to particular embodiments, the second passivation layer **40** may include a layer of silicon nitride, and the first passivation layer **30** may include a layer of aluminum oxide.

[0041] In some embodiments, the second passivation layer **40** may be sufficiently thick so that a surface of the second passivation layer opposite the substrate is substantially higher than the top surface **20B** of the mesa **20** relative to the substrate **12.** In an alternative, a combined thickness of the first and second passivation layers **30** and **40** may be greater than a thickness of the mesa **20** to a degree sufficient to provide mechanical stability and protection to the mesa **20.** According to particular embodiments, the first passivation layer may have a thickness in the range of approximately 0.1 to 2 microns, and the second passivation layer **40** may have a thickness in the range of approximately 0.1 to 5 microns.

[0042] The ohmic contact **26** may be formed on the mesa surface **20B** before or after forming either of the first and/or second passivation layers **30** and **40.** The ohmic contact layer **26** may extend across a substantial entirety of a width of the mesa surface **20B** between mesa sidewalls **20A,** and/or portions of the first passivation layer **30** may extend on portions of the ohmic contact layer **26** opposite the substrate. In an alternative, portions of the first passivation layer **30** may extend directly on the mesa surface, and/or portions of the ohmic contact layer may extend on portions of the first passivation layer **30** opposite the mesa surface **20B.**

[0043] A via **42** through the second passivation layer **40** may expose portions of the ohmic contact layer **26** and portions of the first passivation layer **30** adjacent the ohmic contact layer **26.** The metal overlayer **50** may extend across the second passivation layer **40,** exposed portions of the first passivation layer **30,** and/or exposed portions of the ohmic contact layer **26.** Accordingly, the metal overlayer **50** may contact the ohmic contact **26** through the via **42.** The metal overlayer **50** may include a layer of a metal such as nickel, gold, platinum, titanium, tungsten, molybdenum, tantalum, palladium, and/or combinations thereof.

[0044] In addition, the via **42** may have a width that is greater than a width of the mesa surface **20B** so that sidewalls of the via **42** are spaced apart from the mesa sidewalls **20A.** According to particular embodiments, the via **42** may have a width in the range of approximately 5 to 15 microns. Accordingly, stress and/or pressure applied to a surface of the passivation layer **40** may be directed away from the mesa **20.** Moreover, portions of the passivation layer **30** exposed by the via **42** and the mesa **20** may be shielded from external stresses by the surrounding second passivation layer **40.**

[0045] According to particular embodiments of the present invention, a semiconductor device may include a semiconductor structure, such as epitaxial semiconductor structure **14,** defining a mesa **20** having a mesa surface **20B** opposite the substrate **12** and mesa sidewalls **20A** between the mesa surface **20B** and the substrate **12.** A first passivation layer **30** may be provided on at least portions of the mesa sidewalls **20A** and on the substrate **12** adjacent the mesa sidewalls **20A** wherein at least a portion of the mesa surface **20B** is free of the first passivation layer **30.** A second passivation layer **40** may be provided on the first passivation layer **30** wherein at least a portion of the mesa surface **20B** is free of the second passivation layer **40.** Moreover, the first and second passivation layers may comprise different materials. In addition, a metal overlayer may be provided on the second passivation layer **40,** on portions of the first passivation layer **30** free of the second passivation layer **40,** and on portions of the mesa surface **20B** free of the first and second passivation layers. An ohmic contact layer **26** may be provided between the metal overlayer 50 and the mesa surface **20B,** and the ohmic contact layer **26** and the metal overlayer **50** may comprise different materials.

[0046] According to additional embodiments of the present invention, a semiconductor device may include a semiconductor structure **14** on substrate **12,** the semiconductor structure **14** defining a mesa surface **20B** and mesa sidewalls **20A** between the mesa surface **20B** and the substrate **12.** A passivation layer may be provided on the mesa sidewalls **20A** and on the substrate **12** adjacent the mesa sidewalls with the passivation layer having a via therein so that at least a portion of the mesa surface is free of the passivation layer. More particularly, the via in the passivation layer may define a stair-step profile such that a first portion V_1 of the via hole has a first width W_1 and a second portion of the via hole V_2 has a second width

[0047] W_2 different than the first width W_1. In addition, the via hole may include a plateau region P between the first and second portions of the via hole, and the plateau region P may be substantially parallel with the substrate **12.** More particularly, the second width W_2 may be greater than the first width W_1. In addition, the second width W_2 may be greater than a width of the mesa surface **20B,** and the first width W_1 may be less than a width of the mesa surface **20B.** According to some embodiments, the passivation layer may include a layer of a single material patterned to provide the stair-step profile. In an alternative, the passivation layer may include first and second passivation layers **30** and **40** of different materials so that the second passivation layer **40** can be selectively etched relative to the first passivation layer **30.**

[0048] Methods of fabricating semiconductor devices according to embodiments of the present invention are illustrated in Figures 2A-2D. In particular, an epitaxial semiconductor structure **14** can be formed on a substrate **12,** with the epitaxial semiconductor structure **14** including a mesa **20** having mesa sidewalls **20A** and a mesa surface **20B.** The epitaxial semiconductor structure **14**

may be formed by forming a uniformly thick epitaxial semiconductor layer and then selectively removing portions of the epitaxial semiconductor layer to form the mesa **20**. Portions of the epitaxial semiconductor layer may be selectively removed using a wet or dry etch such as a reactive ion etch (RIE), an electron cyclotron resonance (ECR) plasma etch, and/or an inductively coupled plasma (ICP) etch. For example, the mesa **20** may be patterned using a dry etch in an argon (Ar) environment using a chlorine (Cl_2) etchant. More particularly, the dry etch may include flowing argon (Ar) in the range of approximately 2 to 40 sccm and flowing chlorine (Cl_2) in the range of approximately 5 to 50 sccm in an RIE reactor at a pressure at a pressure in the range of approximately 5 to 50 mTorr and at an RF power in the range of approximately 200 to 1000 W. While particular etch conditions have been provided by way of example, other etch conditions may be used.

[0049] As shown, only a portion of the epitaxial semiconductor structure **14** may be included in the mesa **20**. In an alternative, all of the epitaxial semiconductor structure **14** may be included in the mesa **20** so that mesa sidewalls **20A** may extend to the substrate **12**. The epitaxial semiconductor structure **14** may include an N-type layer on the substrate and a P-type layer on the N-type layer opposite the substrate. The mesa **20** may include portions of the N-type layer and none of the P-type layer; all of the N-type layer and portions (but not all) of the P-type layer; or all of the N-type and P-type layers (such that sidewalls of the mesa **20** extend to the substrate **12**).

[0050] The epitaxial semiconductor structure **14** may also include an active layer between N-type and P-type layers. An active layer may include a number of different structures and/or layers and/or combinations thereof. The active layer, for example, may include single or multiple quantum wells, double heterostructures, and/or superlattices. An active layer may also include light and/or current confinement layers that may encourage laser action in the device.

[0051] A first passivation layer **30** may be formed on sidewalls **20A** of the mesa **20** and on portions of the substrate **12** adjacent the mesa sidewalls **20A**. As shown, if the mesa sidewalls **20A** do not extend to the substrate **12**, portions of the semiconductor structure **14** may remain between the first passivation layer **30** and the substrate adjacent the mesa sidewalls **20A**. The first passivation layer **30** may be a layer or multiple sublayers of an insulating material such as silicon nitride, silicon dioxide, aluminum oxide, and/or combinations thereof. Moreover, the first passivation layer **30** may be formed using a deposition technique such as plasma enhanced chemical vapor deposition, low pressure chemical vapor deposition, chemical vapor deposition, sputtering, e-beam evaporation, and/or combinations thereof. According to particular embodiments, the first passivation layer **30** may be a layer of aluminum oxide, and the first passivation layer **30** may have a thickness in the range of approximately 0.1 to 2 microns.

[0052] The first passivation layer **30** may include a via **32** therein to provide electrical contact to the mesa surface **20B**. The via **32**, for example, may be formed according to steps discussed in U.S. Patent Application Serial No. (Attorney Docket No. 5308-280) filed concurrently herewith, and in U.S. Patent Application Serial No. (Attorney Docket No. 5308-281) filed concurrently herewith. For example, the passivation layer **30** may be formed on the mesa surface **20B** and then patterned using photolithography to form the via **32** exposing portions of the mesa surface, and after forming the via **32**, an ohmic contact layer can be formed on the exposed portion of the mesa surface (either before or after forming a second passivation layer). In an alternative, an ohmic contact layer may be formed on the mesa surface prior to forming the passivation layer, the passivation layer can be formed over the ohmic contact layer, and portions of the passivation layer on the ohmic contact layer can be removed. In another alternative, an ohmic contact layer can be formed on the mesa surface, and a mask used to pattern the ohmic contact layer can be maintained while forming the first passivation layer. The mask and portions of the passivation layer on the mask can be removed thereby exposing portions of the ohmic contact layer without requiring a separate mask.

[0053] As shown in Figure 2B, a second passivation layer **40** can be formed on the first passivation layer **30**. The second passivation layer **40** may include a layer or multiple sublayers of an insulating material such as silicon nitride, silicon dioxide, and/or aluminum oxide, and the second passivation layer may be formed using a deposition technique such as plasma enhanced chemical vapor deposition, low pressure chemical vapor deposition, chemical vapor deposition, sputtering, e-beam evaporation, and/or combinations thereof.

[0054] The first passivation layer **30** may comprise a first material, and the second passivation layer **40** may comprises a second material different than the first material. Accordingly, an etchant may be selected so that the second passivation layer **40** can be etched without significantly etching the first passivation layer **30** when forming a via through the second passivation layer **40**. According to particular embodiments, the first passivation layer **30** may comprise a layer of aluminum oxide, and the second passivation layer **40** may comprise a layer of silicon nitride. Accordingly, the a via hole can be etched through the second passivation layer **40** to expose portions of the first passivation layer without significantly etching the second passivation layer.

[0055] As shown in Figure 2C, a via **42** can be opened in the second passivation layer **40** by masking portions of the second passivation layer to be maintained (by means such as photolithography) and etching exposed portions of the second passivation layer. If the via through the first passivation layer **20** has been previously formed, the via **42** may expose portions of the mesa surface **20B** without further processing. In an alternative, a via through the first passivation layer **30** may be formed after forming

the via **42** through the second passivation layer **40**.

[0056] According to particular embodiments, the via **42** may be formed in the second passivation layer by masking portions of the second passivation layer and etching the exposed portions of the second passivation layer using a reactive ion etch (RIE). More particularly, the RIE etch can be performed using a fluorine-based etch chemistry such as NF_2 and/or CHF_3. which may be used to etch silicon nitride selectively with respect to aluminum oxide. Other etch chemistries may be used provided that the etch chemistry exhibits selectivity in etching the material of the second passivation layer with respect to the material of the first passivation layer. Etch chemistries based on NF_2 and/or CHF_3, for example, may selectively etch silicon nitride at a much higher rate that aluminum oxide. Accordingly, an aluminum oxide first passivation layer **30** may effectively act as an etch stop when etching the via **42** through a silicon nitride second passivation layer **40**.

[0057] Once portions of the mesa surface **20B** and the first passivation layer **30** have been exposed by the via **42**, an ohmic contact **26** may be formed on the exposed portion of the mesa surface **20B** as shown in Figure 2D. In alternatives, the ohmic contact layer may be formed before forming the first passivation layer **20B**, or between forming the first and second passivation layers **30** and **40**. A metal overlayer **50** can then be formed on the on the second passivation layer **40**, on exposed portions of the first passivation layer **30** in the via, and on the ohmic contact layer **26** in the via. According to some embodiments, the ohmic contact layer and the metal overlayer may comprise respective layers of the same or different metals. In an alternative, a separate ohmic contact layer may not be required so that the metal overlayer is formed directly on exposed portions of the mesa surface **20B**.

[0058] A second ohmic contact layer **27** may also be formed on the substrate **12** opposite the semiconductor structure **14** to provide a "vertical" current path between the ohmic contact layers **26** and **27**. While the ohmic contact layer **27** is shown as being formed after patterning the first and second passivation layers **30** and **40**, the ohmic contact layer **27** may be formed at an earlier stage of fabrication. Moreover, a second ohmic contact layer may instead be formed on a same side of the substrate **12** as the first ohmic contact layer **26** to thereby provide a "horizontal" current flow.

[0059] According to embodiments of the present invention, a first passivation layer **30** may provide protection and/or insulation for sidewalls **20A** of a semiconductor mesa **20**, and a surface **20B** of the semiconductor mesa may be exposed through the first passivation layer **30** to provide a relatively precise pattern. Stated in other words, a pattern having a width less than a width of the mesa surface **20B** may be formed in the first passivation layer **30** to expose portions of the mesa surface **20B** and/or an ohmic contact layer **26** thereon. A second passivation layer **40** can be formed on the first passivation layer **30**, and the second passivation layer **40** can be patterned with a relatively imprecise pattern to expose the mesa surface **20B** and/or an ohmic contact layer **26** thereon, and to expose portions of the first passivation layer **30** adjacent the mesa surface **20B**. Stated in other words, a pattern of the second passivation layer **40** may have a width that is significantly greater than a width of the mesa surface **20B**. Accordingly, the second passivation layer **40** may provide protection for the mesa **20** without requiring precise alignment of patterning for the second passivation layer **40**.

[0060] Figure 3 is a scanning electron microscope (SEM) photomicrograph of a structure according to embodiments of the present invention. More particularly, Figure 3 is a photomicrograph of a laser diode structure according to embodiments of the present invention including a silicon carbide substrate **112** and an epitaxial semiconductor structure **114** comprising Group III-nitride compound semiconductor materials. Portions of the semiconductor structure **114** have been patterned into a mesa **120** and may provide optical and/or current confinement. An ohmic contact layer **126** is provided on a surface of the mesa **120** opposite the substrate **112**. A first passivation layer **130** of aluminum oxide may protect and/or insulate surfaces of the epitaxial semiconductor structure **114**, and a second passivation layer **140** of silicon nitride is provided on the first passivation layer **130**. A via **142** through the second passivation layer **140** exposes a portion of ohmic contact **126**, and metal overlayer **150** provides electrical contact with ohmic contact layer **126** through the via **142**.

[0061] Figure 4 is a cross sectional view illustrating structures according to additional embodiments of the present invention. As shown, the structure may include a substrate **212**, a semiconductor structure **214**, an ohmic contact layer **226**, and a first passivation layer **230** on the semiconductor structure and on portions of the ohmic contact layer **226**. More particularly, the semiconductor structure **214** may include a mesa **220** having mesa sidewalls **220A** and a mesa surface **220B**, and the ohmic contact layer **226** may include sidewalls **226A** and a contact surface **226B**. In embodiments illustrated in Figure 4, the ohmic contact layer **226** can be formed before forming the passivation layer **230** so that portions of the first passivation layer **230** extend on portions of the ohmic contact layer **226**.

[0062] A second passivation layer **240** is provided on the first passivation layer, and a via **242** in the second passivation layer **240** may expose the contact surface of the ohmic contact layer **226** and portions of the first passivation layer **230** adjacent the ohmic contact layer **226**. A width of the via **242** in the second passivation layer **240** may be significantly greater than a width of the mesa surface **220B**. In addition, a metal overlayer **250** may be provided on the second passivation layer **240**, on exposed portions of the first passivation layer **230**, and on the contact surface **226B** of the ohmic contact layer **226**. In addition, an ohmic contact layer **227** may be provided on the substrate **212** opposite the mesa **220**.

[0063] The semiconductor structure **214** may include a Group III-V compound semiconductor material such as a Group **III-nitride** compound semiconductor material. Moreover, the semiconductor structure **214** may include an N-type layer on the substrate and a P-type layer on the N-type layer opposite the substrate **212**. In addition, the mesa **220** may include portions of the P-type layer and none of the N-type layer; all of the P-type layer and portions (but not all) of the N-type layer; or all of the P-type and N-type layers (such that sidewalls **220A** extend to the substrate **212**).

[0064] In some embodiments, the substrate **212** may include substrate materials such as N-type silicon carbide having a polytype such as 2H, 4H, 6H, 8H, 15R, and/or 3C; sapphire; gallium nitride; and/or aluminum nitride. Moreover, the substrate **212** may be conductive to provide a "vertical" device having a "vertical" current flow through the epitaxial semiconductor structure **214** and the substrate **212**. In an alternative, the substrate **212** may be insulating or semi-insulating where both ohmic contacts are provided on a same side of the substrate to provide a "horizontal" device. A conductive substrate could also be used in a "horizontal" device. Moreover, the term substrate may be defined to include a non-patterned portion of the semiconductor material making up the semiconductor structure **214**, and/or there may not be a material transition between the substrate **212** and the semiconductor structure **214**.

[0065] Figures 5A-D are cross-sectional views illustrating steps of forming structures illustrated in Figure 4. As shown in Figure 5A, a semiconductor structure **214** including a mesa **220** may be formed on a substrate **212**, and an ohmic contact layer **226** may be formed on a surface **220B** of the mesa. A passivation layer **230** can then be formed on sidewalls **220A** of the mesa **220**, on portions of the substrate adjacent the mesa sidewalls **220A** and on portions of the ohmic contact layer **226**. As shown in Figure 5A, the passivation layer **230** may extend onto portions of beveled sidewalls **226A** adjacent to the mesa sidewalls **220A** while the contact surface **226B** and portions of the beveled sidewalls **226A** adjacent to the contact surface **226B** are maintained free of the passivation layer **230**. In an alternative, portions of the passivation layer **230** may extend onto surface portions of the ohmic contact layer parallel with the substrate.

[0066] The mesa **220** and the ohmic contact layer **226**, for example, may be formed using a single patterning step as discussed, for example, in U.S Application Serial No._____ (Attorney Docket No. 5308-281). More particularly, a semiconductor layer of uniform thickness may be formed, a contact metal layer may be formed on the semiconductor layer of uniform thickness, and a mask may be formed on the contact metal layer. The contact metal layer and the semiconductor layer can then be etched using the single mask to form the ohmic contact layer **226** and the mesa **220**. Moreover, the mask may be maintained while forming the first passivation layer **230**, and the mask and portions of the first passivation layer on the mask can be removed to expose the contact surface **226B** of the ohmic contact layer. Accordingly, a single mask may provide alignment of the ohmic contact layer with the mesa surface, and the single mask may provide alignment of a "via" through the passivation layer exposing the contact surface **226A** of the ohmic contact layer **226**.

[0067] In an alternative, the ohmic contact layer **226** and/or the passivation layer **230** may be patterned using a separate masking operation(s). For example, the mesa **220** and the ohmic contact layer **226** may be patterned using a first mask, and a via may be patterned in the passivation layer **230** using a second mask. In another alternative, the mesa **220** may be patterned using a first mask, the ohmic contact layer **226** may be patterned using a second mask, and a via may be patterned in the passivation layer **230** using a third mask.

[0068] As shown in Figure 5B, a second passivation layer **240** can be formed on the first passivation layer **230** and on exposed portions of the ohmic contact layer **226**. Each of the first a second passivation layers **230** and **240** may comprise a layer of an insulting material such as silicon nitride, silicon dioxide, and/or aluminum oxide. Moreover, each of the first and second passivation layers **230** and **240** may comprise a different material such that the second passivation layer **230** can be etched using an etch chemistry that is selective with respect to the first passivation layer **240**. For example, the first passivation layer **230** may comprises a layer of aluminum oxide, the second passivation layer **240** may comprise a layer of silicon nitride, and a fluorine based etch chemistry may be used to etch the second passivation layer **240** without etching the first passivation layer **230**.

[0069] As shown in Figure 5C, the second passivation layer **240** may be patterned to expose the contact surface **226B** of the ohmic contact layer **226**, and to expose portions of the first passivation layer **230** adjacent the ohmic contact layer **226**. A width of the via **242** in the passivation layer **240** may be significantly greater than a width of the mesa surface **220B**. More particularly, the mesa surface **220A** may have a width in the range of approximately 1 to 3 microns, and the via **242** through passivation layer **240** may have a width in the range of approximately 5 to 15 microns. Accordingly, a high degree of precision may not be required when patterning the via **242** in the passivation layer **240**. As shown in Figure 5D, a metal overlayer **250** can be formed on the passivation layer **240**, on exposed portions of the first passivation layer **230**, and on exposed portions of the ohmic contact layer **226**.

[0070] According to embodiments of the present invention, a first passivation layer may provide relatively precise exposure of an ohmic contact layer on a semiconductor mesa (or exposure of a surface of the semiconductor mesa) and protection of sidewalls of the mesa. A second passivation layer of a different material may provide structural protection for the mesa without requiring a high degree of precision in the patterning thereof.

[0071] Semiconductor devices discussed above may

provide edge emitting semiconductor lasers with light being emitted parallel to the substrate along a lengthwise direction of a semiconductor mesa stripe. Stated in other words, the light may be emitted along a direction perpendicular to the cross sections of figures discussed above. While methods and devices have been discussed with reference to methods of forming light emitting devices such as laser diodes, methods according to embodiments of the present invention may be used to form other semiconductor devices such as conventional diodes, conventional light emitting diodes, or any other semiconductor device including a semiconductor mesa.

[0072] While this invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the scope of the invention as defined by the appended claims and their equivalents.

Claims

1. A method of forming a semiconductor device, the method comprising:

   forming a semiconductor structure (14) on a substrate (12), the semiconductor structure (14) defining a mesa (20) having a mesa surface (20B) and mesa sidewalls (20A) between the mesa surface (20) and the substrate (12); and
   forming a passivation layer on the mesa sidewalls (20A) and on the substrate (12) adjacent the mesa sidewalls (20A), the passivation layer (40) having a via hole (42) therein so that at least a portion of the mesa surface (20B) is free of the passivation layer, **characterised in that** the via hole (42) defines a stair-step profile such that a first portion (V_1) of the via hole (42) has a first width (W_1) and a second portion (V_2) of the via hole (42) has a second width (W_2) different than the first width (W_1).

2. A method according to Claim 1 wherein the stair-step profile includes a plateau region (P) between the first (V_1) and second (V_2) portions of the via hole (42) having the first (W_1) and second (W_2) widths.

3. A method according to Claim 2 wherein the plateau portion (P) is substantially parallel to the substrate (12).

4. A method according to Claim 1 wherein the first portion (V_1) of the via hole (42) having the first width (W_1) is between the second portion (V_2) of the via hole (42) having the second width (W_2), and the mesa surface (20B), and wherein the second width (W_2) is greater than the first width (W_1).

5. A method according to Claim 1 wherein the passivation layer comprises a first layer (30) of a first material and second layer (40) of a second material different than the first material and wherein the first portion (V_1) of the via hole (42) is through at least a portion of the first layer (30) and wherein the second portion (V_2) of the via hole (42) is through at least a portion of the second layer (40).

6. A method according to Claim 5 wherein forming the passivation layer comprises etching the second layer (40) of the second material using an etch chemistry that etches the second material of the second layer (40) preferentially with respect to the first material of the first layer (30).

7. A method according to Claim 6 wherein the first portion (V_1) of the via hole (42) is formed through at least the portion of the first layer (30) before forming the second layer (40) of the second material.

8. A method according to Claim 6 wherein the first portion (V_1) of the via hole (42) is formed through at least the portion of the first layer (30) after forming the second layer (40) of the second material.

9. A method according to Claim 5 wherein a thickness of the first passivation layer (30) is greater than a thickness of the mesa (20).

10. A method according to Claim 5 wherein the first material comprises aluminum oxide.

11. A method according to Claim 5 wherein the second material comprises silicon nitride.

12. A method according to Claim 1 further comprising:

    forming a contact layer (26,27) on the at least a portion of the mesa surface (20B) free of the passivation layer.

13. A method according to Claim 12 further comprising:

    forming a metal layer (50) on the contact layer (26,27) and on at least portions of the passivation layer.

14. A method according to Claim 13 wherein the contact layer (26,27) and the metal layer (50) comprises different materials.

15. A method according to Claim 12 wherein a portion of the passivation layer extends on a portion of the contact layer (26,27) opposite the mesa surface (20B).

16. A method according to Claim 12 wherein the contact

layer (26,27) extends onto at least a portion of the passivation layer opposite the substrate (12).

17. A method according to Claim 1 wherein the semiconductor structure includes a P-type layer and an N-type layer wherein at least a portion of the P-type layer and/or the N-type layer is included in the mesa.

18. A semiconductor device comprising:

a substrate (12);
a semiconductor structure on the substrate (12), the semiconductor structure defining a mesa (20) having a mesa surface (20B) and mesa sidewalls (20A) between the mesa surface (20B) and the substrate (12); and
a passivation layer on the mesa sidewalls (20A) and on the substrate (12) adjacent the mesa sidewalls (20A), the passivation layer having a via hole (42) therein so that at least a portion of the mesa surface (20B) is free of the passivation layer, **characterised in that** the via hole (42) defines a stair-step profile such that a first portion (V_1) of the via hole (42) has a first width (W_1) and a second portion (V_2) of the via hole (42) has a second width (W_2) different than the first width (W_1).

19. A semiconductor device according to Claim 18 wherein the stair-step profile includes a plateau region (P) between the first (V_1) and second (V_2) portions of the via hole (42) having the first and second widths.

20. A semiconductor device according to Claim 19 wherein the plateau portion (P) is substantially parallel to the substrate (12).

21. A semiconductor device according to Claim 18 wherein the first portion (V_1) of the via hole (42) having the first width (W_1) is between the second portion (V_2) of the via hole (42), having the second width (W_2) and the mesa surface (20B) and wherein the second width (W_2) is greater than the first width (W_1).

22. A semiconductor device according to Claim 18 wherein the passivation layer comprises a first layer (30) of a first material and second layer (40) of a second material different than the first material and wherein the first portion (V_1) of the via hole (42) is through at least a portion of the first layer (30) and wherein the second portion (V_2) of the via hole (42) is through at least a portion of the second layer (40).

23. A semiconductor device according to Claim 22 wherein a thickness of the first passivation layer is greater than a thickness of the mesa.

24. A semiconductor device according to Claim 22 wherein the first material comprises aluminum oxide.

25. A semiconductor device according to Claim 22 wherein the second material comprises silicon nitride.

26. A semiconductor device according to Claim 22 wherein the second material comprises a material that can be etched preferentially with respect to the first material using a predetermined etch chemistry.

27. A semiconductor device according to Claim 18 further comprising:

a contact layer (26,27) on the at least a portion of the mesa surface (20B) free of the passivation layer.

28. A semiconductor device according to Claim 27 further comprising a metal layer (50) on the contact layer (26,27) and on at least portions of the passivation layer.

29. A semiconductor device according to Claim 28 wherein the contact layer (26,27) and the metal layer (50) comprise different materials.

30. A semiconductor device according to Claim 27 wherein a portion of the passivation layer extends on a portion of the contact layer (26,27) opposite the mesa surface (20B).

31. A semiconductor device according to Claim 27 wherein the contact layer (26,27) extends onto at least a portion of the passivation layer opposite the substrate (12).

32. A semiconductor device according to Claim 18 wherein the semiconductor structure includes a P-type layer and an N-type layer wherein at least a portion of the P-type layer and/or the N-type layer is included in the mesa.

Patentansprüche

1. Verfahren zur Herstellung einer Halbleitervorrichtung, wobei das Verfahren aufweist:

Bilden einer Halbleiterstruktur (14) auf einem Substrat (12), wobei die Halbleiterstruktur (14) eine Mesa (20) definiert, welche eine Mesaoberfläche (20B) und Mesaseitenwände (20A) zwischen der Mesaoberfläche (20) und dem Substrat (12) aufweist und
Bilden einer Passivierungsschicht auf den Mesaseitenwänden (20A) und auf dem Substrat

(12) neben den Mesaseitenwänden (20A), wobei die Passivierungsschicht (40) ein Durchgangsloch (42) darin aufweist, so daß mindestens ein Teil der Mesaoberfläche (20B) frei von der Passivierungsschicht ist, **dadurch gekennzeichnet, daß** das Durchgangsloch (42) ein Treppenstufenprofil definiert, so daß ein erster Teil (V_1) des Durchgangslochs (42) eine erste Breite (W_1) aufweist und ein zweiter Teil (V_2) des Durchgangslochs (42) eine zweite Breite (W_2) aufweist, die von der ersten Breite (W_1) verschieden ist.

2. Verfahren nach Anspruch 1, **dadurch gekennzeichnet, daß** das Treppenstufenprofil einen Plateaubereich (P) zwischen den ersten (V_1) und zweiten (V_2) Teilen des Durchgangslochs (42), welche die ersten (W_1) und zweiten (W_2) Breiten aufweisen, aufweist.

3. Verfahren nach Anspruch 2, **dadurch gekennzeichnet, daß** der Plateaubereich (P) im wesentlichen parallel zu dem Substrat (12) ist.

4. Verfahren nach Anspruch 1, **dadurch gekennzeichnet, daß** der erste Teil (V_1) des Durchgangslochs (42), welcher die erste Breite (W_1) aufweist, zwischen dem zweiten Teil (V_2) des Durchgangslochs (42), das die zweite Breite (W_2) aufweist, und der Mesaoberfläche (20B) liegt und wobei die zweite Breite (W_2) größer ist als die erste Breite (W_1).

5. Verfahren nach Anspruch 1, **dadurch gekennzeichnet, daß** die Passivierungsschicht eine erste Schicht (30) aus einem ersten Material und eine zweite Schicht (40) aus einem zweiten Material, welches von dem ersten Material verschieden ist, aufweist und wobei der erste Teil (V_1) des Durchgangslochs (42) durch mindestens einen Teil der ersten Schicht (30) geht und wobei der zweite Teil (V_2) des Durchgangsloch (42) durch mindestens einen Teil der zweiten Schicht (40) geht.

6. Verfahren nach Anspruch 5, **dadurch gekennzeichnet, daß** das Bilden der Passivierungsschicht ein Ätzen der zweiten Schicht (40) aus dem zweiten Material aufweist, wobei eine Ätzchemie verwendet wird, welche das zweite Material der zweiten Schicht (40) bevorzugt gegenüber dem ersten Material der ersten Schicht (30) ätzt.

7. Verfahren nach Anspruch 6, **dadurch gekennzeichnet, daß** der erste Teil (V_1) des Durchgangslochs (42) durch mindestens den Teil der ersten Schicht (30) gebildet wird bevor die zweite Schicht (40) aus dem zweiten Material gebildet wird.

8. Verfahren nach Anspruch 6, **dadurch gekennzeichnet, daß** der erste Teil (V_1) des Durchgangslochs (42) durch mindestens den Teil der ersten Schicht (30) gebildet wird nach dem Bilden der zweiten Schicht (40) aus dem zweiten Material.

9. Verfahren nach Anspruch 5, **dadurch gekennzeichnet, daß** eine Dicke der ersten Passivierungsschicht (30) größer ist als eine Dicke der Mesa (20).

10. Verfahren nach Anspruch 5, **dadurch gekennzeichnet, daß** das erste Material Aluminiumoxid aufweist.

11. Verfahren nach Anspruch 5, **dadurch gekennzeichnet, daß** das zweite Material Siliciumnitrid aufweist.

12. Verfahren nach Anspruch 1 darüber hinaus mit:

    Bilden einer Kontaktschicht (26, 27) auf mindestens einem Teil der von der Passivierungsschicht freien Mesaoberfläche (20B).

13. Verfahren nach Anspruch 12 darüber hinaus mit:

    Bilden einer Metallschicht (50) auf der Kontaktschicht (26, 27) und mindestens auf Teilen der Passivierungsschicht.

14. Verfahren nach Anspruch 13, **dadurch gekennzeichnet, daß** die Kontaktschicht (26, 27) und die Metallschicht (50) verschiedene Materialien aufweisen.

15. Verfahren nach Anspruch 12, **dadurch gekennzeichnet, daß** sich ein Teil der Passivierungsschicht auf einen Teil der Kontaktschicht (26, 27) gegenüber der Mesaoberfläche (20B) erstreckt.

16. Verfahren nach Anspruch 12, **dadurch gekennzeichnet, daß** sich die Kontaktschicht (26, 27) auf mindestens einen Teil der Passivierungsschicht gegenüber dem Substrat (12) erstreckt.

17. Verfahren nach Anspruch 1, **dadurch gekennzeichnet, daß** die Halbleiterstruktur eine Schicht vom P-Typ und eine Schicht vom N-Typ aufweist, wobei mindestens ein Teil der Schicht vom P-Typ und/oder der Schicht vom N-Typ in der Mesa enthalten ist.

18. Halbleitervorrichtung mit:

    einem Substrat (12),
    einer Halbleiterstruktur auf dem Substrat (12), wobei die Halbleiterstruktur eine Mesa (20) definiert, welche eine Mesaoberfläche (20B) und Mesaseitenwände (20A) zwischen der Mesao-

berfläche (20B) und dem Substrat (12) aufweist und
einer Passivierungsschicht auf den Mesaseitenwänden (20A) und dem Substrat (12) neben den Mesaseitenwänden (20A), wobei die Passivierungsschicht ein Durchgangsloch (42) darin aufweist, und wobei mindestens ein Teil der Mesaoberfläche (20B) frei von der Passivierungsschicht ist, **dadurch gekennzeichnet, daß** das Durchgangsloch (42) ein Treppenstufenprofil aufweist, so daß ein erster Teil (V_1) des Durchgangslochs (42) eine erste Breite (W_1) aufweist und ein zweiter Teil (V_2) des Durchgangslochs (42) eine zweite Breite (W_2) aufweist, die von der ersten Breite (W_1) verschieden ist.

19. Halbleitervorrichtung nach Anspruch 18, **dadurch gekennzeichnet, daß** das Treppenstufenprofil einen Plateaubereich (P) aufweist zwischen ersten (V_1) und zweiten (V_2) Teilen des Durchgangslochs (42), welche die ersten und zweiten Breiten aufweisen.

20. Halbleitervorrichtung nach Anspruch 19, **dadurch gekennzeichnet, daß** der Plateaubereich (P) im wesentlichen parallel zu dem Substrat (12) ist.

21. Halbleitervorrichtung nach Anspruch 18, **dadurch gekennzeichnet, daß** der erste Teil (V_1) des Durchgangslochs (42), welches die erste Breite (W_1) aufweist, zwischen dem zweiten Teil (V_2) des Durchgangslochs (42), das die zweite Breite (W_2) aufweist, und der Mesaoberfläche (20B) liegt und wobei die zweite Breite (W_2) größer ist als die erste Breite (W_1).

22. Halbleitervorrichtung nach Anspruch 18, **dadurch gekennzeichnet, daß** die Passivierungsschicht eine erste Schicht (30) aus einem ersten Material und eine zweite Schicht (40) aus einem zweiten Material, das von dem ersten Material verschieden ist, aufweist und wobei der erste Teil (V_1) des Durchgangslochs (42) durch mindestens einen Teil der ersten Schicht (30) geht und wobei der zweite Teil (V_2) des Durchgangslochs (42) durch mindestens einen Teil der zweiten Schicht (40) geht.

23. Halbleitervorrichtung nach Anspruch 22, **dadurch gekennzeichnet, daß** eine Dicke der ersten Passivierungsschicht größer ist als eine Dicke der Mesa.

24. Halbleitervorrichtung nach Anspruch 22, **dadurch gekennzeichnet, daß** das erste Material Aluminiumoxid aufweist.

25. Halbleitervorrichtung nach Anspruch 22, **dadurch gekennzeichnet, daß** das zweite Material Siliciumnitrid aufweist.

26. Halbleitervorrichtung nach Anspruch 22, **dadurch gekennzeichnet, daß** das zweite Material ein Material aufweist, das gegenüber dem ersten Material bevorzugt geätzt werden kann, wobei eine vorbestimmte Ätzchemie verwendet wird.

27. Halbleitervorrichtung nach Anspruch 18 darüber hinaus mit:

einer Kontaktschicht (26, 27) auf dem mindestens einen von der Passivierungsschicht freien Teil der Mesaoberfläche (20B).

28. Halbleitervorrichtung nach Anspruch 27 darüber hinaus mit einer Metallschicht (50) auf der Kontaktschicht (26, 27) und mindestens auf Teilen der Passivierungsschicht.

29. Halbleitervorrichtung nach Anspruch 28, **dadurch gekennzeichnet, daß** die Kontaktschicht (26, 27) und die Metallschicht (50) verschiedene Materialien aufweisen.

30. Halbleitervorrichtung nach Anspruch 27, **dadurch gekennzeichnet, daß** sich ein Teil der Passivierungsschicht auf einen Teil der Kontaktschicht (26, 27) gegenüber der Mesaoberfläche (20B) erstreckt.

31. Halbleitervarrichturtg nach Anspruch 27, **dadurch gekennzeichnet, daß** sich die Kontaktschicht (26, 27) auf mindestens einen Teil der Passivierungsschicht gegenüber dem Substrat (12) erstreckt.

32. Halbleitervorrichtung nach Anspruch 18, **dadurch gekennzeichnet, daß** die Halbleiterstruktur eine Schicht vom P-Typ und eine Schicht vom N-Typ aufweist, wobei mindestens ein Teil der Schicht vom P-Typ und/oder der Schicht vom N-Typ in der Mesa enthalten ist.

Revendications

1. Procédé pour former un dispositif semi-conducteur, le procédé comprenant :

former une structure de semi-conducteur (14) sur un substrat (12), la structure de semi-conducteur (14) définissant un mesa (20) ayant une surface mesa (20B) et des parois latérales mesas (20A) entre la surface mesa (20) et le substrat (12) ; et
former une couche de passivation sur les parois latérales mesas (20A) et le substrat (12) adjacent aux parois latérales mesas (20A), la couche de passivation (40) ayant un trou d'interconnexion (42) de sorte qu'au moins une partie de la surface mesa (20B) est sans couche de pas-

sivation, **caractérisé en ce que** le trou d'interconnexion (42) définit un profil crénelé de sorte qu'une première partie (V_1) du trou d'interconnexion (42) comporte une première largeur (W_1) et une seconde partie (V_2) du trou d'interconnexion (42) comporte une seconde largeur (W_2) différente de la première largeur (W_1).

2. Procédé selon la revendication 1, dans lequel le profil crénelé inclut une région plateau (P) entre les première (V_1) et seconde (V_2) parties du trou d'interconnexion (42) ayant les première (W_1) et seconde (W_2) largeurs.

3. Procédé selon la revendication 2, dans lequel la partie plateau (P) est substantiellement parallèle au substrat (12).

4. Procédé selon la revendication 1, dans lequel la première partie (V_1) du trou d'interconnexion (42) ayant la première largeur (W_1) est entre la seconde partie (V_2) du trou d'interconnexion (42) ayant la seconde largeur (W_2) et la surface mesa (20B), et dans lequel la seconde largeur (W_2) est plus grande que la première largeur (W_1).

5. Procédé selon la revendication 1, dans lequel la couche de passivation comprend une première couche (30) d'un premier matériau et une seconde couche (40) d'un second matériau différent du premier matériau et dans lequel la première partie (V_1) du trou d'interconnexion (42) est à travers au moins une partie de la première couche (30) et dans lequel la seconde partie (V_2) du trou d'interconnexion (42) est à travers au moins une partie de la seconde couche (40).

6. Procédé selon la revendication 5, dans lequel former la couche de passivation comprend attaquer la seconde couche (40) du second matériau utilisant une attaque chimique qui attaque le second matériau de la seconde couche (40) de préférence par rapport au premier matériau de la première couche (30).

7. Procédé selon la revendication 6, dans lequel la première partie (V_1) du trou d'interconnexion (42) est formée à travers au moins une partie de la première couche (30) avant de former la seconde couche (40) du second matériau.

8. Procédé selon la revendication 6, dans lequel la première partie (V_1) du trou d'interconnexion (42) est formée à travers au moins la partie de la première couche (30) après formation de la seconde couche (40) du second matériau.

9. Procédé selon la revendication 5, dans lequel une épaisseur de la première couche de passivation (30) est supérieure à l'épaisseur du mesa (20).

10. Procédé selon la revendication 5, dans lequel le premier matériau comprend de l'oxyde d'aluminium.

11. Procédé selon la revendication 5, dans lequel le second matériau comprend du nitrure de silicium.

12. Procédé selon la revendication 1, comprenant en outre :

former une couche contact (26, 27) sur la au moins une partie de la surface mesa (20B) sans couche de passivation.

13. Procédé selon la revendication 12, comprenant en outre :

former une couche métallique (50) sur la couche contact (26, 27) et sur au moins des parties de la couche de passivation.

14. Procédé selon la revendication 13, dans lequel la couche contact (26, 27) et la couche métallique (50) comprennent différents matériaux.

15. Procédé selon la revendication 12, dans lequel une partie de la couche de passivation s'étend sur une partie de la couche contact (26, 27) opposée à la surface mesa (20B).

16. Procédé selon la revendication 12, dans lequel la couche contact (26, 27) s'étend sur au moins une partie de la couche de passivation opposée au substrat (12).

17. Procédé selon la revendication 1, dans lequel la structure de semi-conducteur inclut une couche de type P et une couche de type N dans lesquelles au moins une partie de la couche de type P et/ou la couche de type N est incluse dans le mesa.

18. Dispositif semi-conducteur comprenant :

un substrat (12) ;
une structure de semi-conducteur sur le substrat (12), la structure de semi-conducteur définissant un mesa (20) ayant une surface mesa (20B) et des parois latérales mesas (20A) entre la surface mesa (20B) et le substrat (12) ; et
une couche de passivation sur les parois latérales mesas (20A) et sur le substrat (12) adjacent aux parois latérales mesas (20A), la couche de passivation ayant un trou d'interconnexion (42) de façon à ce qu'au moins une partie de la surface mesa (20B) est sans couche de passivation, **caractérisé en ce que** le trou d'interconnexion (42) définit un profil crénelé de sorte

qu'une première partie (V_1) du trou d'interconnexion (42) a une première largeur (W_1) et une seconde partie (V_2) du trou d'interconnexion (42) a une seconde largeur (W_2) différente de la première largeur (W_1).

19. Dispositif de semi-conducteur selon la revendication 18, dans lequel le profil crénelé inclut une région plateau (P) entre les première (V_1) et seconde (V_2) parties du trou d'interconnexion (42) ayant les première et seconde largeurs.

20. Dispositif de semi-conducteur selon la revendication 19, dans lequel la partie plateau (P) est substantiellement parallèle au substrat (12).

21. Dispositif de semi-conducteur selon la revendication 18, dans lequel la première partie (V_1) du trou d'interconnexion (42) ayant la première largeur (W_1) est entre la seconde partie (V_2) du trou d'interconnexion (42) ayant la seconde largeur (W_2) et la surface mesa (20B), et dans lequel la seconde largeur (W_2) est plus grande que la première largeur (W_1).

22. Dispositif de semi-conducteur selon la revendication 18, dans lequel la couche de passivation comprend une première couche (30) d'un premier matériau et une seconde couche (40) d'un second matériau différent du premier matériau et dans lequel la première partie (V_1) du trou d'interconnexion (42) est à travers au moins une partie de la première couche (30) et dans lequel la seconde partie (V_2) du trou d'interconnexion (42) est à travers au moins une partie de la seconde couche (40).

23. Dispositif de semi-conducteur selon la revendication 22, dans lequel une épaisseur de la première couche de passivation (30) est supérieure à une épaisseur du mesa.

24. Dispositif de semi-conducteur selon la revendication 22, dans lequel le premier matériau comprend de l'oxyde d'aluminium.

25. Dispositif de semi-conducteur selon la revendication 22, dans lequel le second matériau comprend du nitrure de silicium.

26. Dispositif de semi-conducteur selon la revendication 22, dans lequel le second matériau comprend un matériau qui peut être attaqué de préférence par rapport au premier matériau en utilisant une attaque chimique prédéterminée.

27. Dispositif de semi-conducteur selon la revendication 18, comprenant en outre :

une couche contact (26, 27) sur au moins une partie de la surface mesa (20B) sans couche de passivation.

28. Dispositif de semi-conducteur selon la revendication 27, comprenant en outre une couche métallique (50) sur la couche contact (26, 27) et sur au moins des parties de la couche de passivation.

29. Dispositif de semi-conducteur selon la revendication 28, dans lequel la couche contact (26, 27) et la couche métallique (50) comprennent différents matériaux.

30. Dispositif de semi-conducteur selon la revendication 27, dans lequel une partie de la couche de passivation s'étend sur une partie de la couche contact (26, 27) opposée à la surface mesa (20B).

31. Dispositif de semi-conducteur selon la revendication 27, dans lequel la couche contact (26, 27) s'étend sur au moins une partie de la couche de passivation opposée au substrat (12).

32. Dispositif de semi-conducteur selon la revendication 18, dans lequel la structure de semi-conducteur inclut une couche de type P et une couche de type N dans lesquelles au moins une partie de la couche de type P et/ou la couche de type N est incluse dans le mesa.

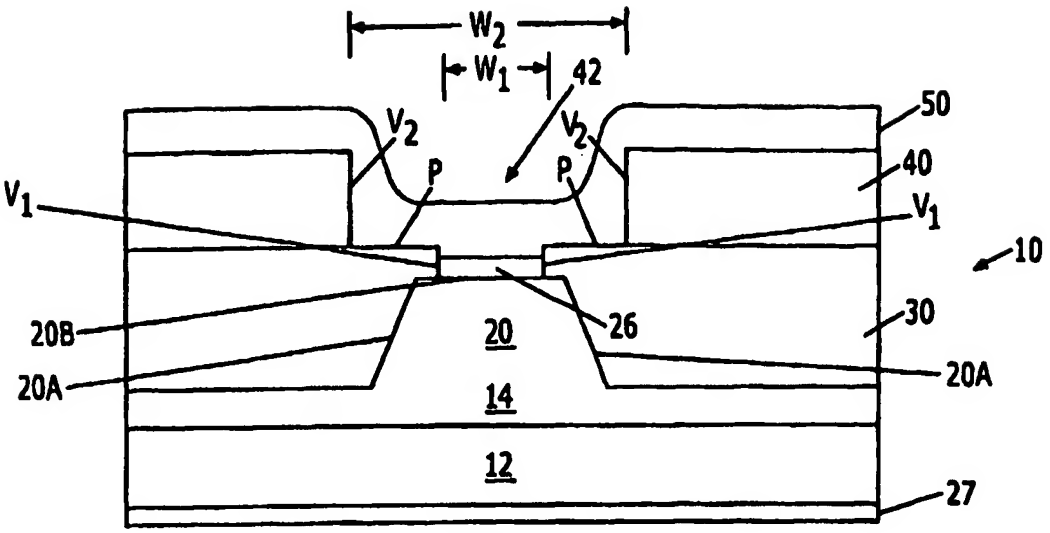


FIG. 1

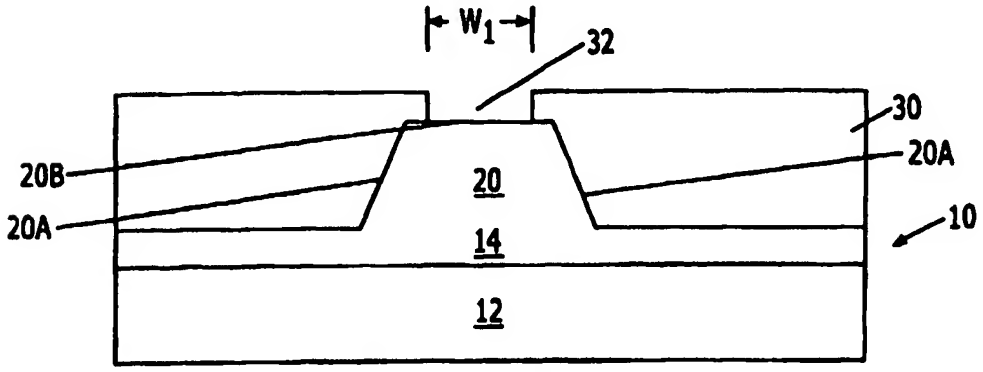


FIG. 2A

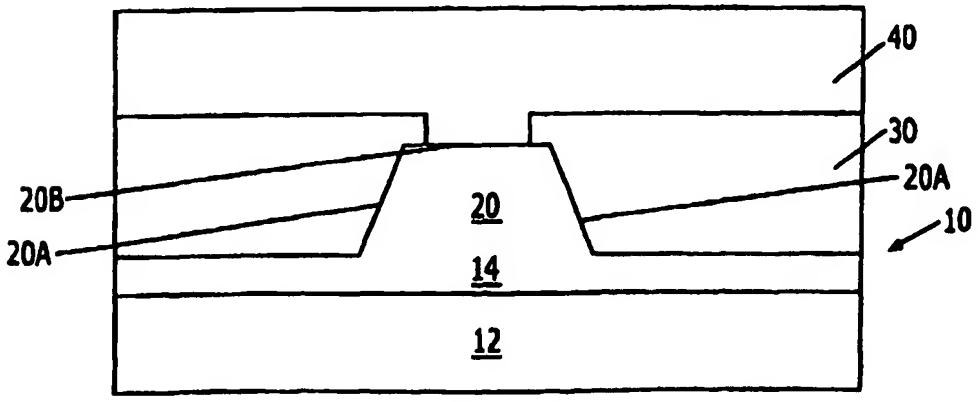


FIG. 2B

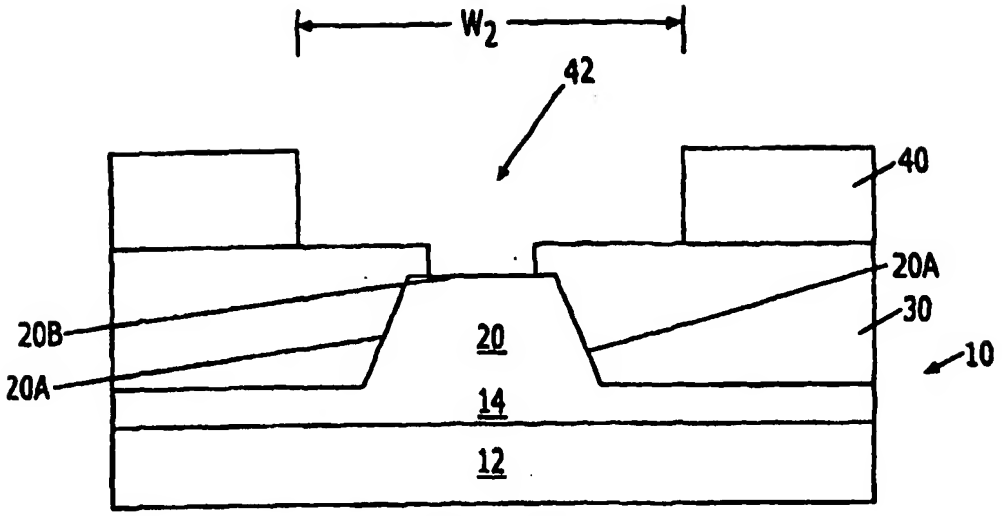

W2
42
40
20A
30
20B
20
10
20A
14
12

FIG. 2C

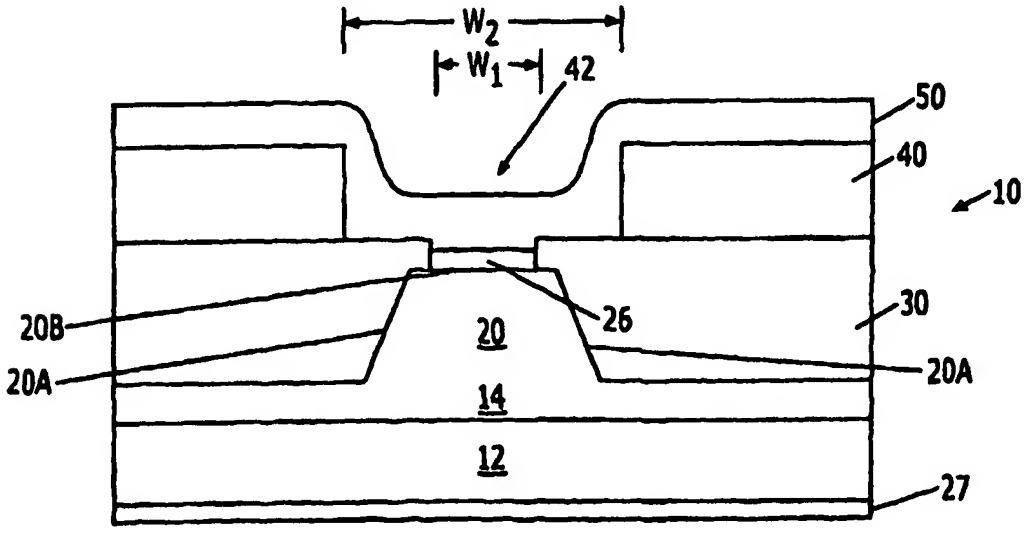

W2
W1
42
50
40
10
20B
26
30
20
20A
20A
14
12
27

FIG. 2D

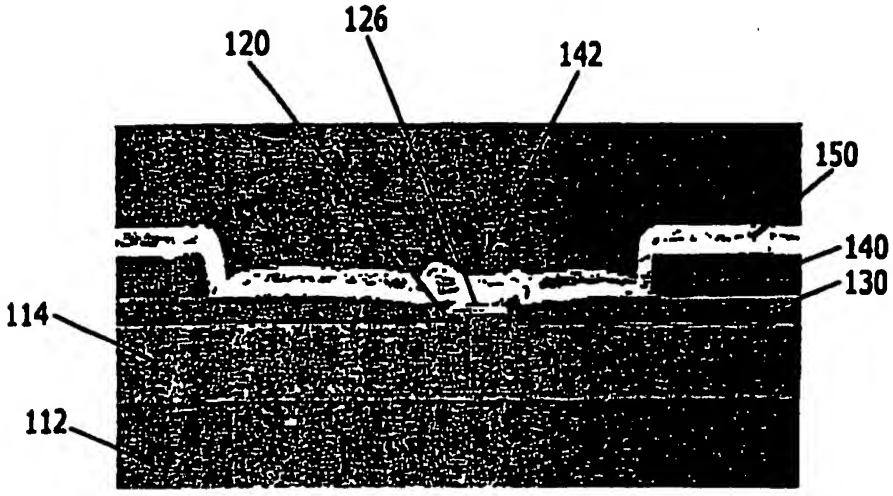


FIG. 3

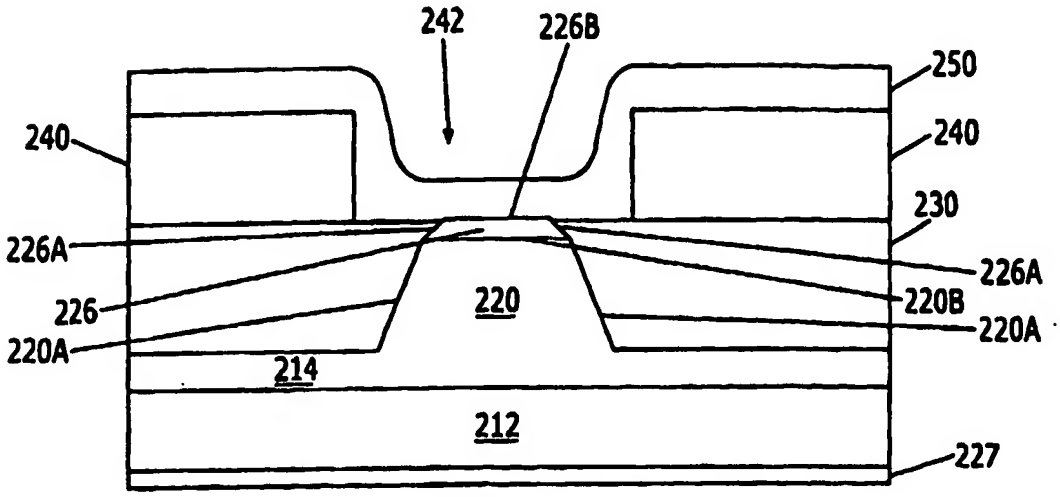


FIG. 4

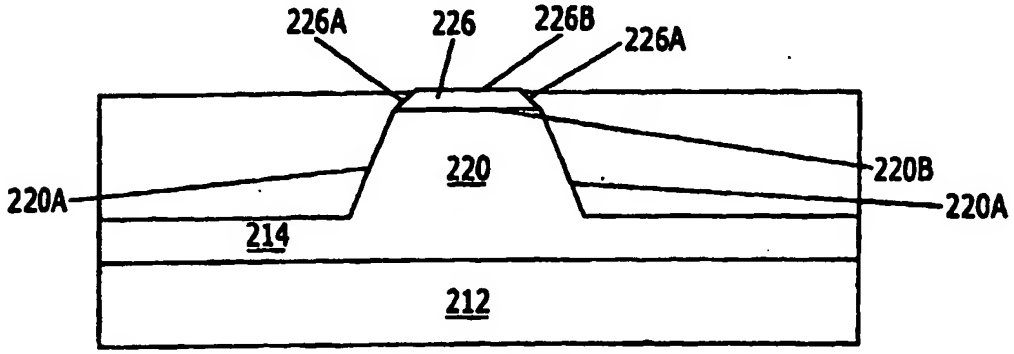


FIG. 5A

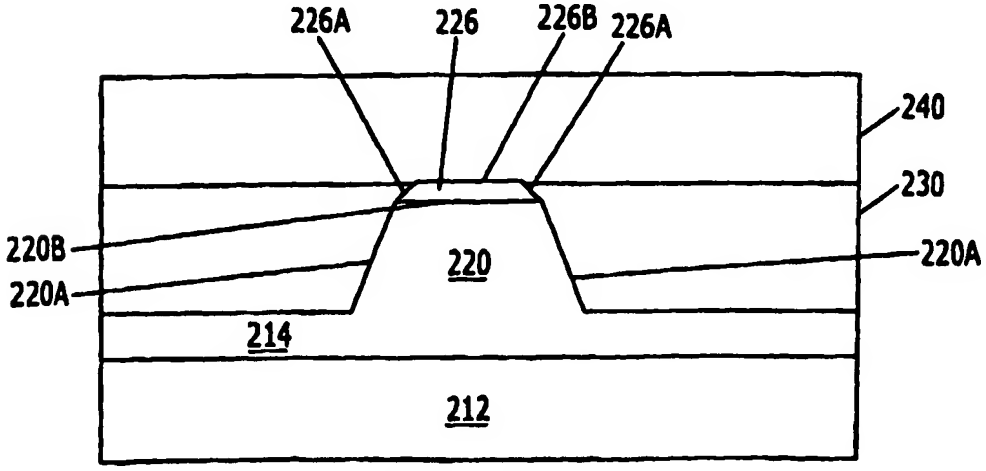
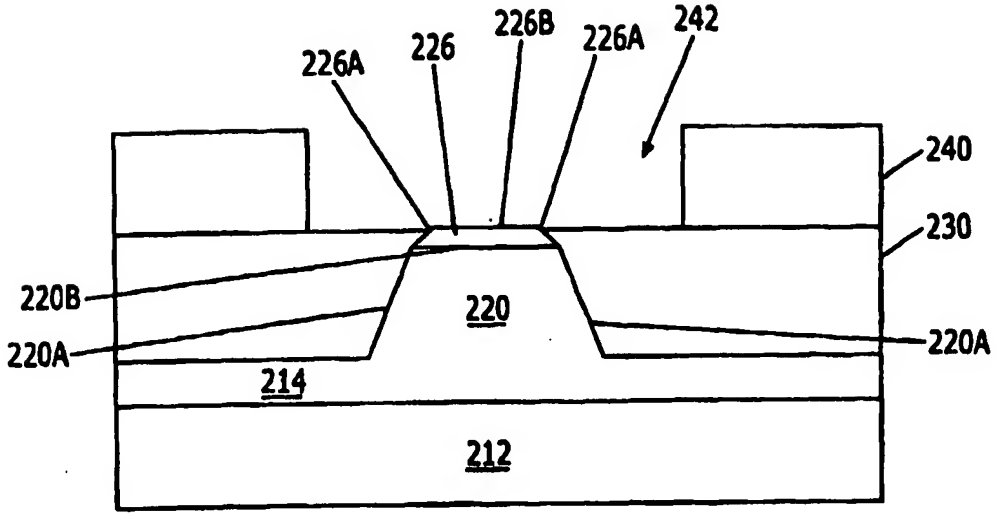


FIG. 5B


226A
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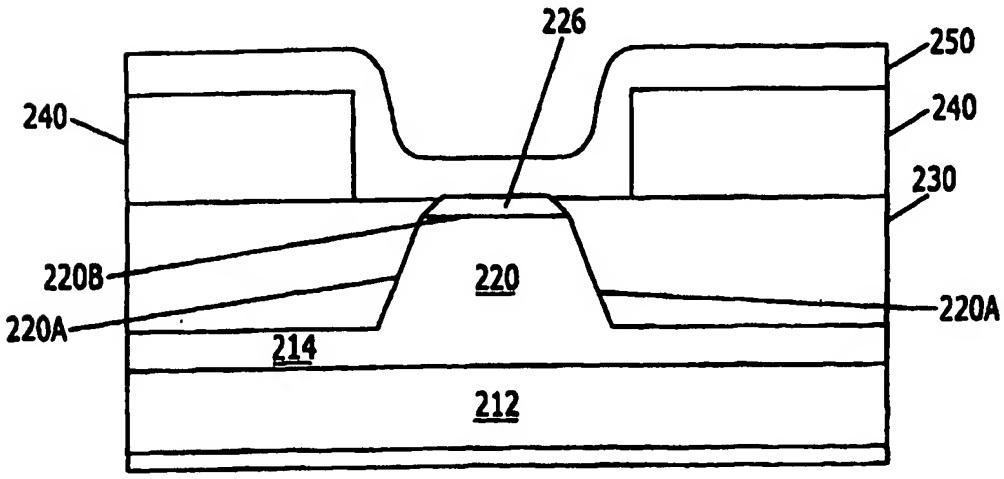
220A
220A
214
212

FIG. 5C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220A
220A
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FIG. 5D